

FIG. 1

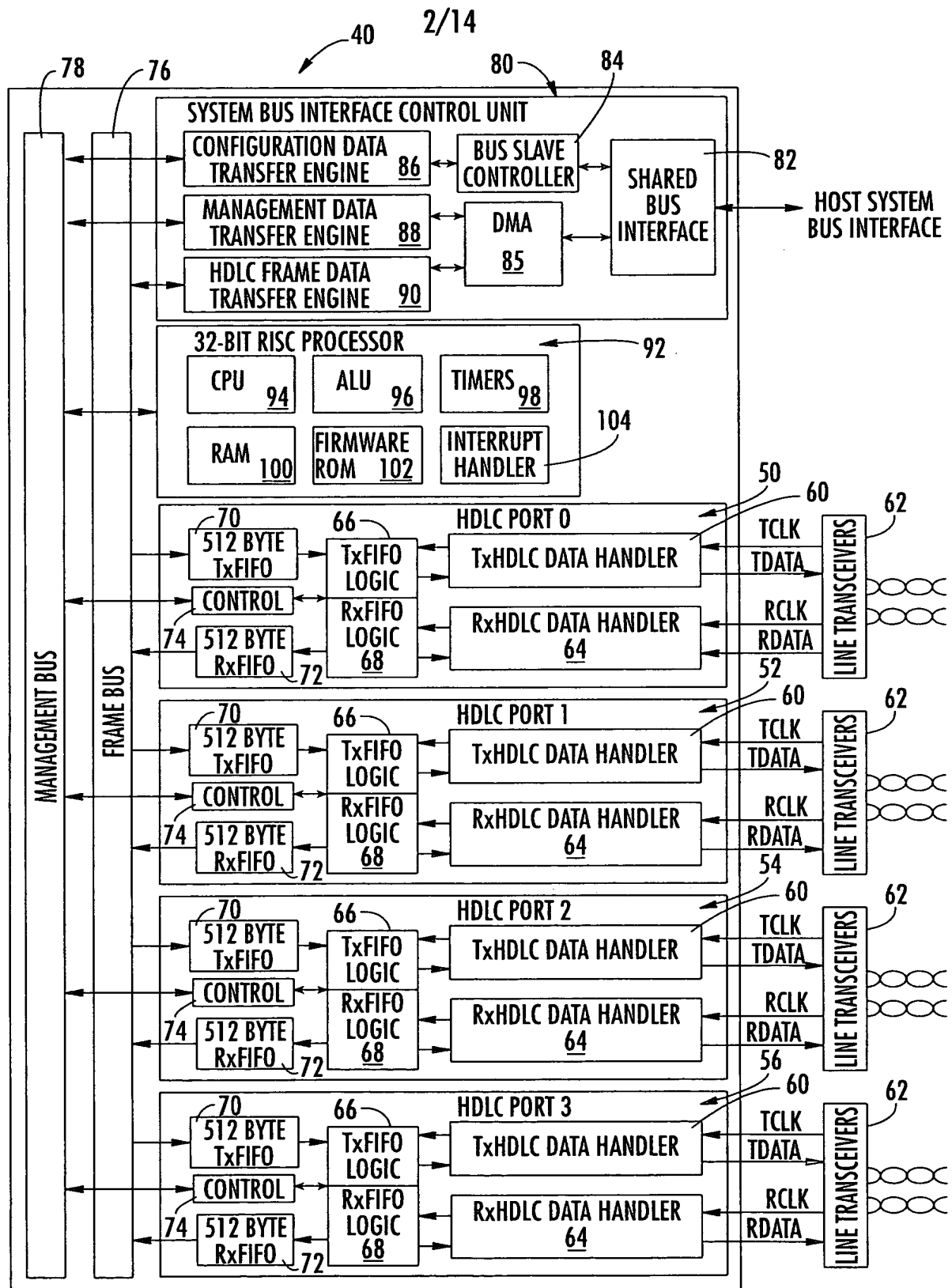


FIG. 2

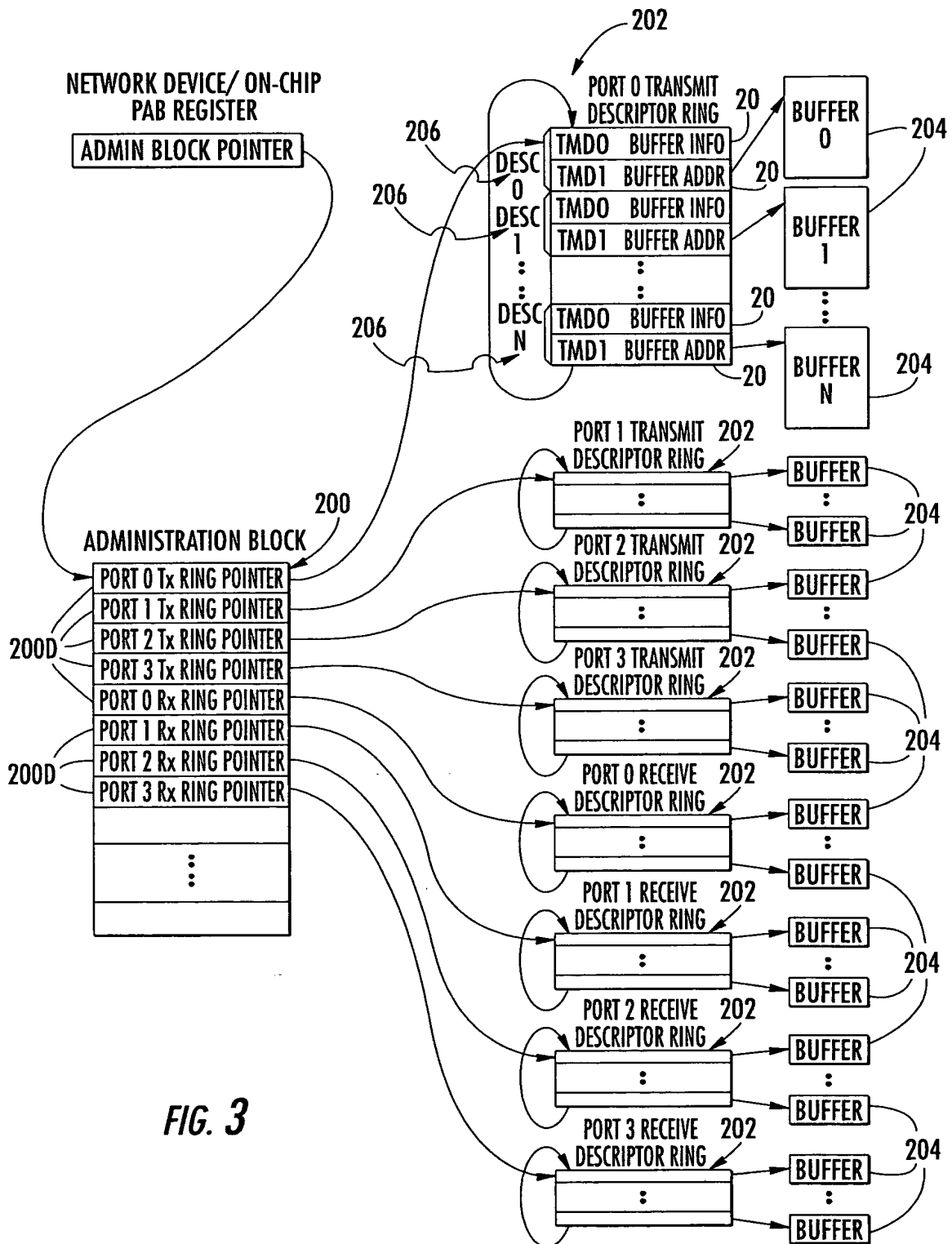


FIG. 3

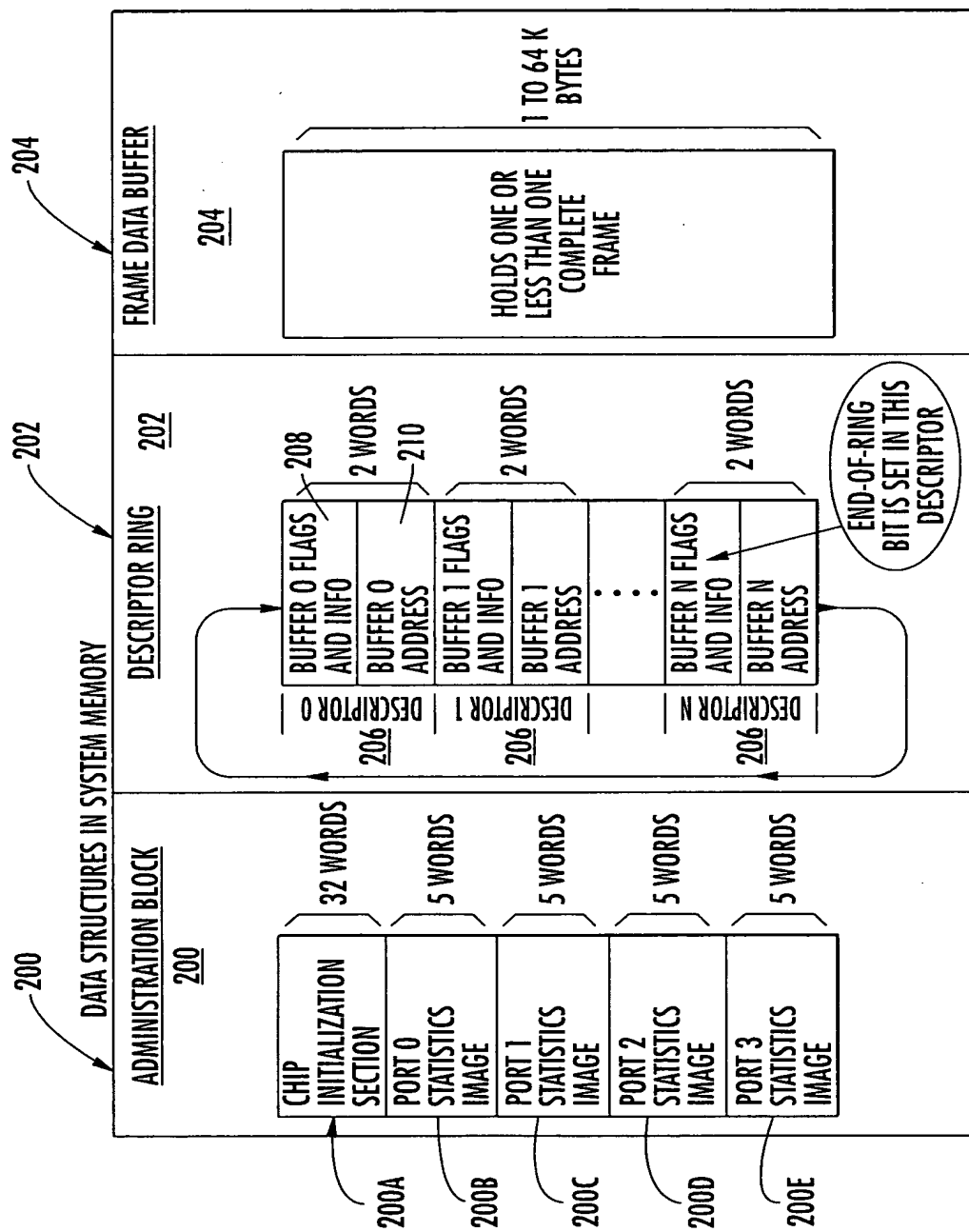


FIG. 4

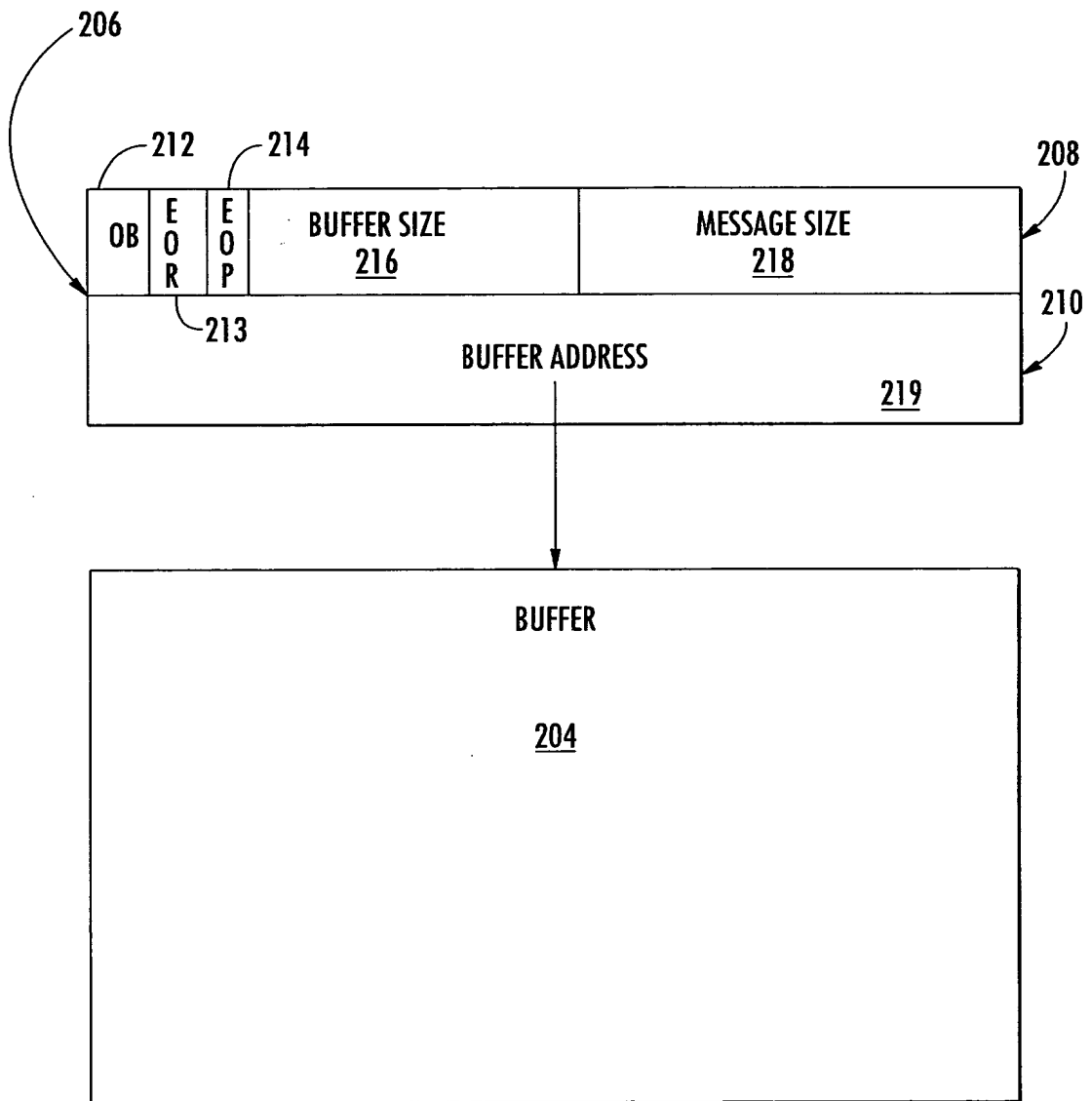
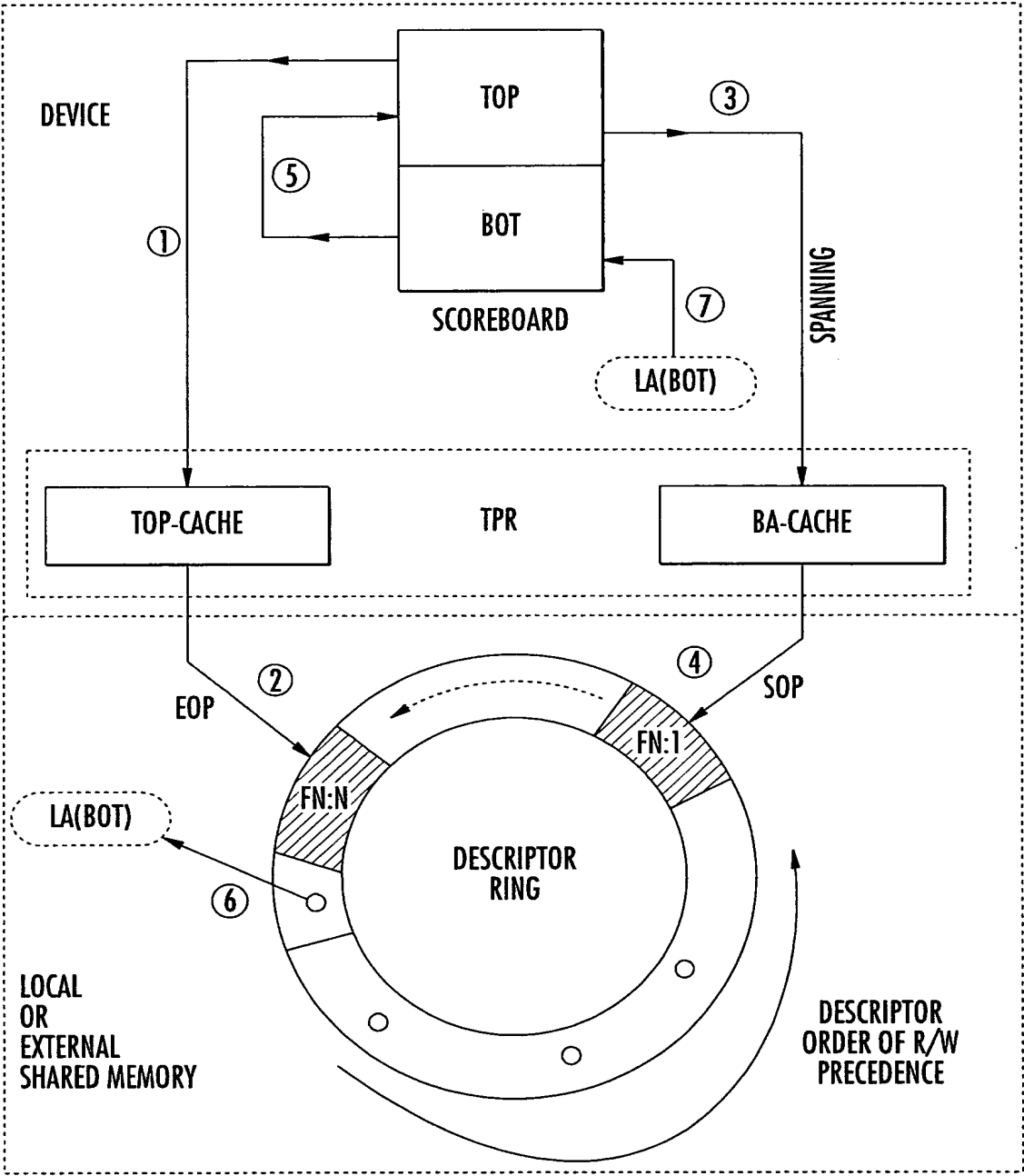


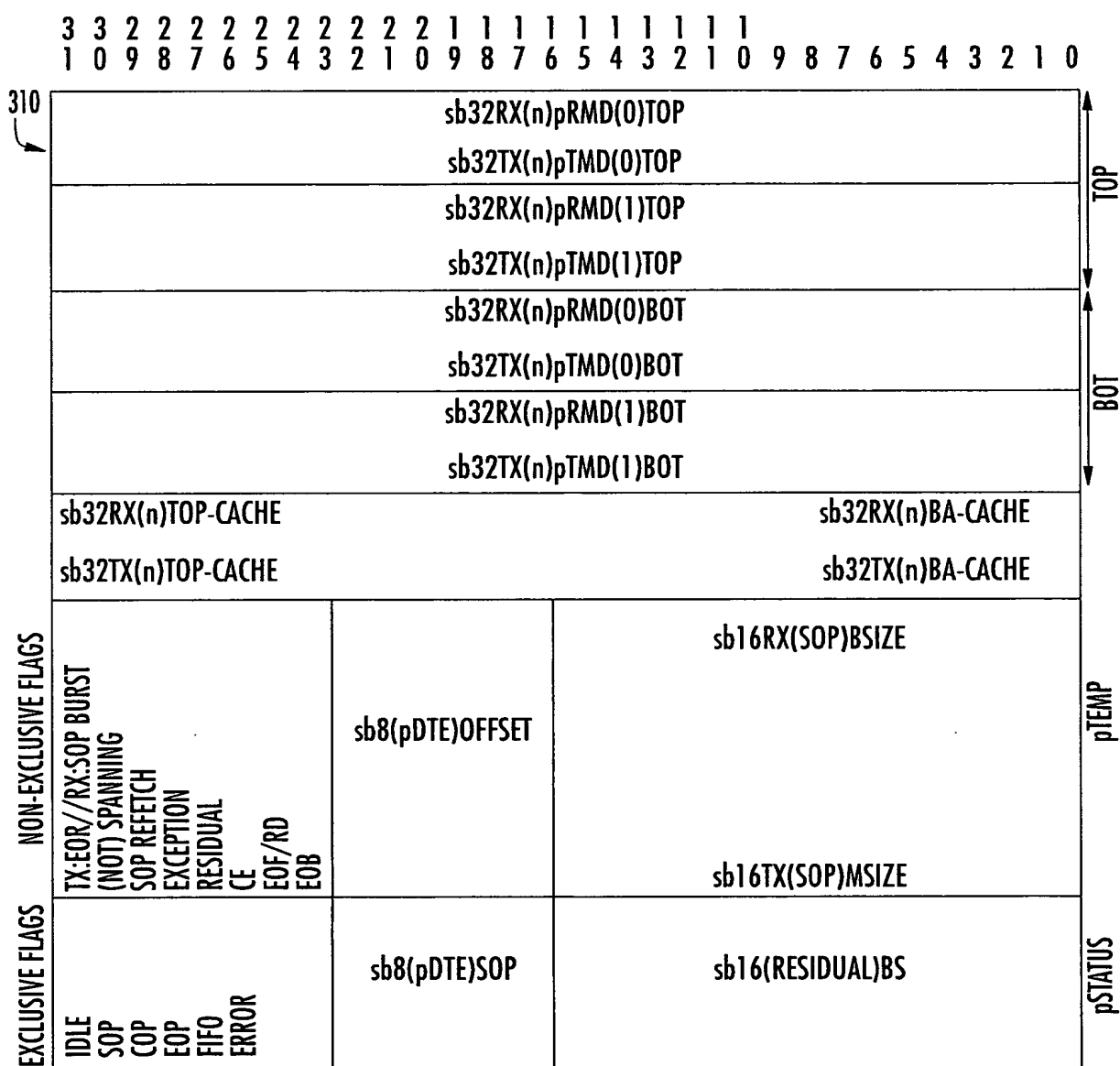
FIG. 5

## FENCEPOST DESCRIPTOR CACHING

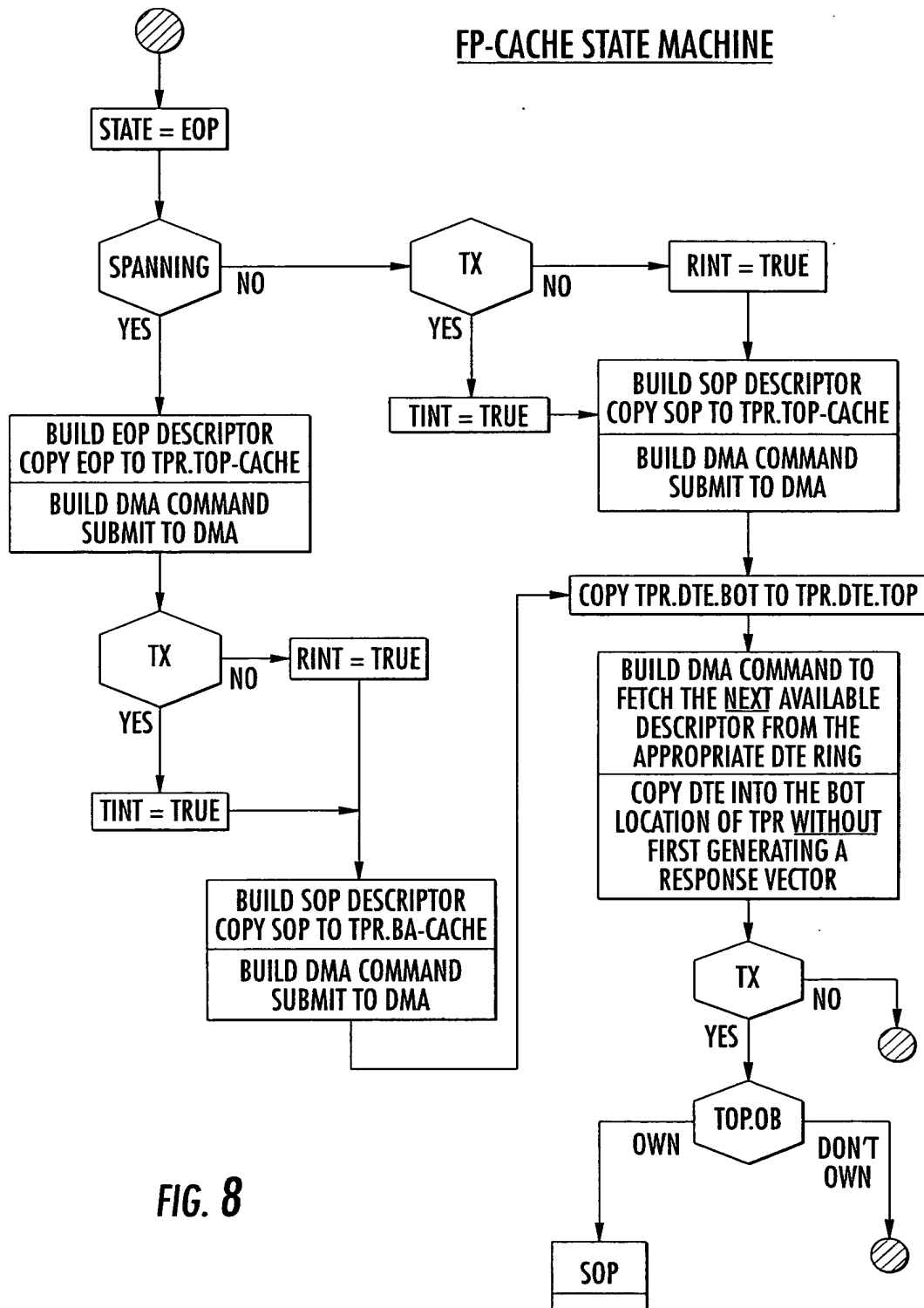


**FIG. 6**

## TPR: SCOREBOARD FORMAT



**FIG. 7**





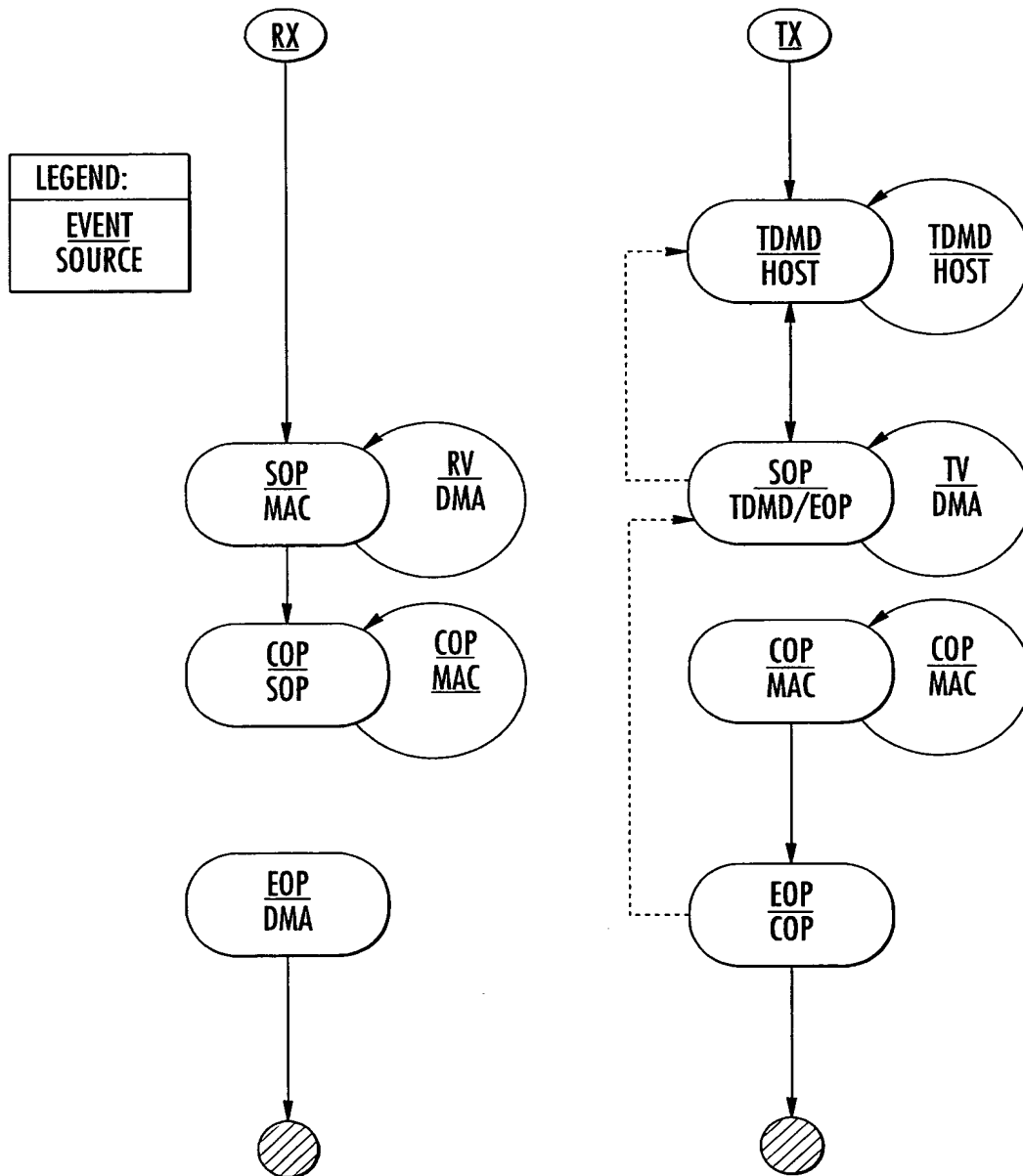
RECEIVE VS TRANSMIT INTERRUPT STATE MACHINES

FIG. 9

# FRAME RECEPTION DIALOG

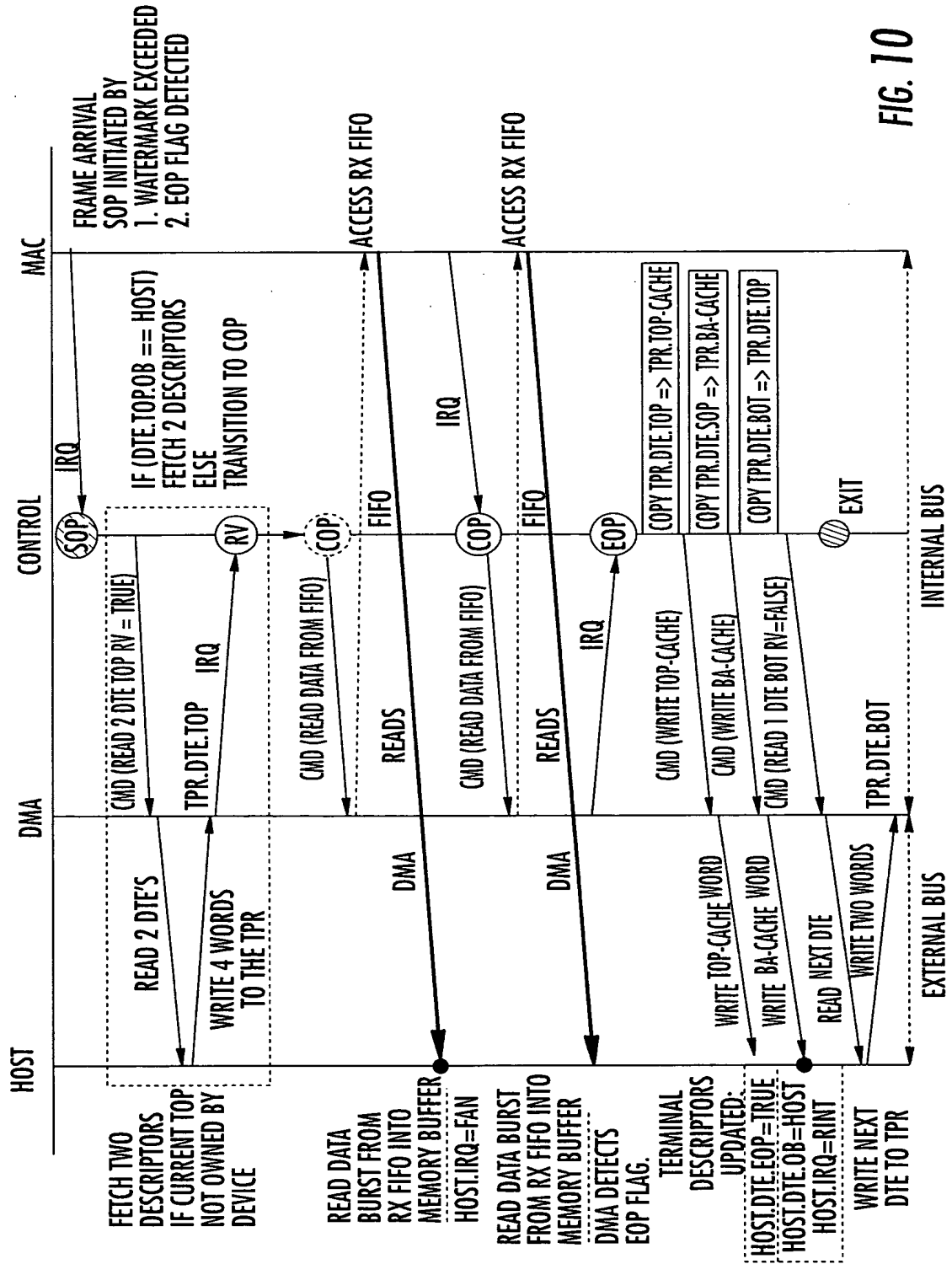


FIG. 10

# FRAME TRANSMISSION DIALOG

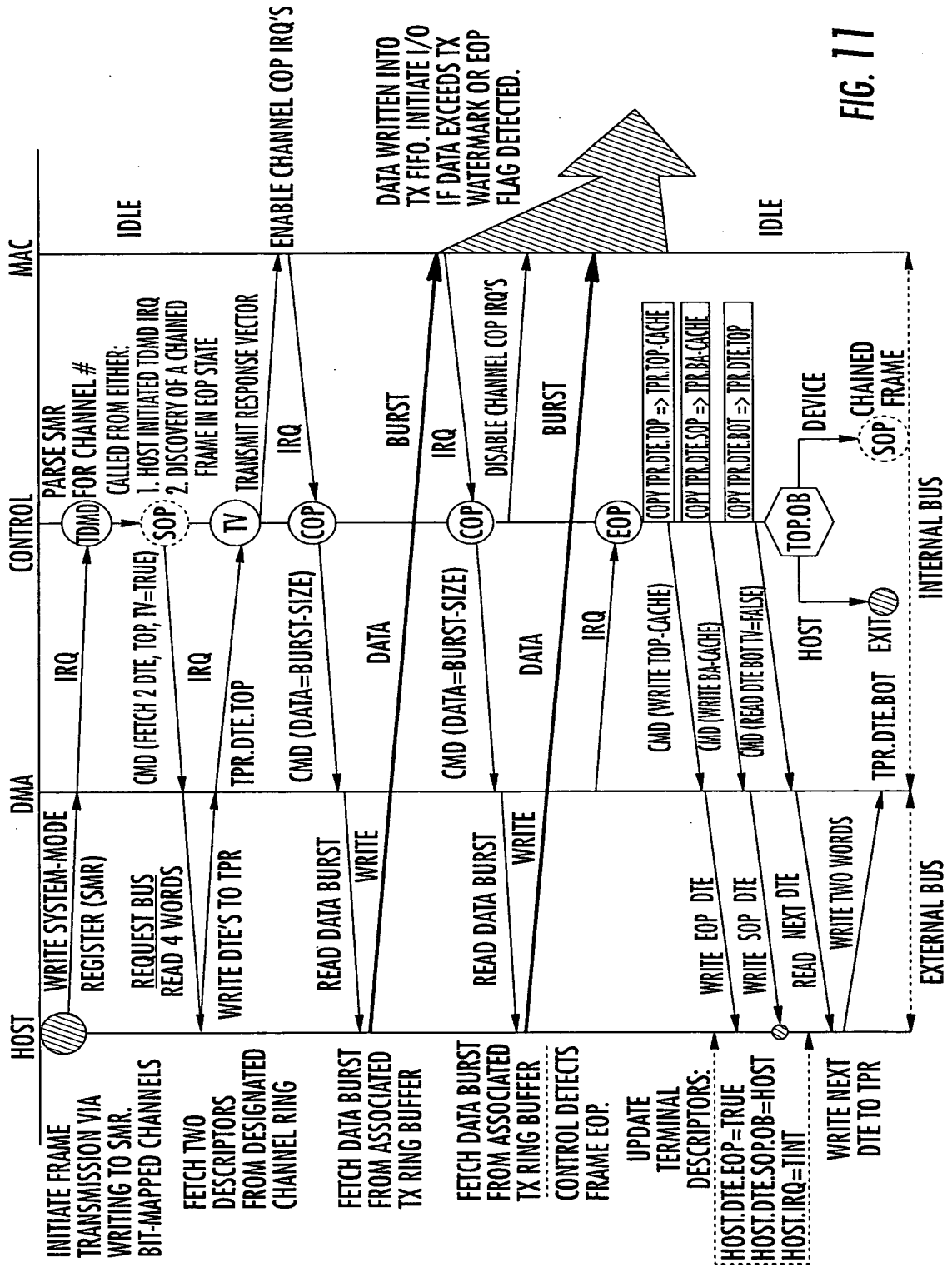


FIG. 11

## [0x31] CMDREG - DMA COMMAND REGISTER

DMA	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT NAME	RESERVED	SFAN	STINT	SRINT	PORT	PORT	PORT	RW	TXERXS	RESMDMD	TYPE	NOCKC	RXSEL	REOC	TXEOPA	TXEOPA	CPC_ADDR[7:0]							XFER_CNT[7:0]								
RESET VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HOST ACCESS	(READ-ZEROS) / (NO-WRITE)																															
HOST UNLOCK	READ-ONLY										READ-ZEROS/WRITE																					
CPC ACCESS	READ-ONLY										READ-ZEROS/WRITE																					

BIT #	FIELD	NAME	DESCRIPTION
31:30	RESERVED	--	THESE BITS ARE NOT IMPLEMENTED
29	SFAN	SET FAN	(1=SET; 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO GENERATE FAN (BIT 27, 19, 11, 3 OF THE REGISTER MIR) UPON COMPLETION OF THE ASSOCIATED COMMAND TRANSFERRING BUFFER OWNERSHIP TO THE HOST. THE DMA SET ONE OF THE FOUR POSSIBLE FAN ACCORDING WITH THE PORT NUMBER SPECIFIED ON THE BITS 26, 25, OF THIS REGISTER.
28	STINT	SET TINT	(1=SET; 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO GENERATE TINT (BIT 25, 17, 9, 1 OF THE REGISTER MIR) UPON COMPLETION OF THE ASSOCIATED COMMAND TRANSFERRING BUFFER OWNERSHIP TO THE HOST. THE DMA SET ONE OF THE FOUR POSSIBLE TINT ACCORDING WITH THE PORT NUMBER SPECIFIED ON THE BITS 26, 25, OF THIS REGISTER.
27	SRINT	SET RINT	(1=SET; 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO GENERATE RINT (BIT 24, 16, 8, 0 OF THE REGISTER MIR) UPON COMPLETION OF THE ASSOCIATED COMMAND TRANSFERRING BUFFER OWNERSHIP TO THE HOST. THE DMA SET ONE OF THE FOUR POSSIBLE TINT ACCORDING WITH THE PORT NUMBER SPECIFIED ON THE BITS 26, 25, OF THIS REGISTER.
26:25	PORT	PORT NUMBER	(11=PORT 3; 10=PORT 2; 01=PORT 1; 00=PORT 0) <i>ONLY FOR FIFO/SYSTEM TRANSFERS.</i> INDICATES THE HDLC PORT NUMBER TO BE USED BY THE DMA FOR FIFO/SYSTEM TRANSFER.
24	RW	SYSTEM MEMORY READ/WRITE	(1=READ; 0=WRITE) <i>USED FOR ALL TRANSFER TYPES.</i> INDICATES THE DIRECTION OF DATA FLOW WITH RESPECT TO SYSTEM MEMORY. WHEN USED FOR FIFO/SYSTEM TRANSFERS THIS FIELD CAN ALSO BE THOUGHT OF AS SELECTING THE Tx- OR Rx-FIFO WITHIN THE HDLC PORT INDICATED IN THE PORT FIELD (Tx=1; Rx=0).
23	TXERXS	Tx END-OF FRAME/ Rx START-OF-FRAME	(1=Tx EOP OR Rx SOP; 0=NORMAL) <i>ONLY USED FOR FIFO/SYSTEM TRANSFERS.</i> SYSTEM-TO-FIFO TRANSFERS (RW=1): INDICATES THIS COMMAND CONSTITUTES THE FINAL TRANSFER OF DATA FOR A GIVEN TRANSMIT FRAME. FIFO-TO-SYSTEM TRANSFERS (RW=0): INDICATES THIS COMMAND IS THE FIRST DATA TRANSFER FOR A GIVEN RECEIVE FRAME.
22	RESMDMD	RESPONSE DEMAND	(1=GENERATE RESPONSE; 0=NO RESPONSE) <i>USED FOR ALL TRANSFER TYPES.</i> ALLOWS THE FIRMWARE TO CONTROL WHETHER OR NOT AN INTERRUPT WILL BE GENERATED FOR THIS COMMAND BY THE DMA. WHEN THIS BIT IS SET THE DMA WILL GENERATES ONE OF THE 8 POSSIBLE INTERRUPTS. EACH INTERRUPT IS RELATIVE TO ONE OF THE 4 PORTS, ACCORDING TO THE PORT NUMBER SPECIFIED ON THE BITS 26,25, AND THE DIRECTION OF THE DATA FLOW SPECIFIED ON THE BIT 24 OF THIS REGISTER.
21	TYPE	TRANSFER TYPE	(1=TPR/SYSTEM TRANSFER; 0=FIFO/SYSTEM TRANSFER) <i>USED FOR ALL TRANSFER TYPES.</i> DETERMINES WHETHER THE DMA WILL PERFORM A TPR/SYSTEM TRANSFER OR A FIFO/SYSTEM TRANSFER.

FIG. 12A

BIT #	FIELD	NAME	DESCRIPTION
20	NOCRC	NO Tx CRC	(1=CRC NOT APPENDED; 0=CRC APPENDED) <i>ONLY FOR SYSTEM-TO-FIFO TRANSFERS WHEN RW=1 AND TXRXS=1.</i> ALLOWS THE FIRMWARE TO CONTROL WHETHER OR NOT THE HDLC TRANSMITTER WILL APPEND A CRC TO THE END OF A GIVEN TRANSMIT FRAME.
19	RXSEL	Rx SELECTION	(1=RX; 0=TX) THIS BIT DISTINGUISH BETWEEN GENERATING THE RX OR THE TX RESPONSE DEMAND INTERRUPT.
18	REOC	REQUEST END OF COMMAND	(1=SET; 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO SET THE BIT 3 OF THE DMASAT AFTER COMPLETION OF THE CURRENT COMMAND.
17:16	TXEOPA	TRANSMIT END-OF-FRAME ALIGNMENT	(11=3 BYTE; 10=2 BYTES; 01=1 BYTE; 00=4 BYTES) <i>ONLY FOR SYSTEM-TO-FIFO TRANSFERS WHEN RW=1 AND TXRXS=1.</i> COMMUNICATES TO THE DMA THE NUMBER OF VALID BYTES IN THE LAST WORD OF A TRANSMIT FRAME TRANSFER.
15:8	CPC_ADDR	CPC ADDRESS	(8-BIT BINARY VALUE) <i>ONLY FOR TPR/SYSTEM TRANSFERS.</i> INDICATES THE STARTING WORD ADDRESS WITHIN THE CPC'S MEMORY. THE DMA HAS NO PROVISION TO PROTECT FROM WRAP-AROUND (0xFF TO 0x00).
7:0	XFER_CNT	TRANSFER COUNT	(8-BIT BINARY VALUE) <i>USED FOR ALL TRANSFER TYPES.</i> INDICATES THE FIRMWARE-REQUESTED NUMBER OF DATA-TRANSFERRING UCLK CYCLES THE DMA WILL PERFORM – KNOWN AS THE “BURST SIZE”. THIS IS THE NUMBER 4-BYTE WORDS THE DMA WILL TRANSFER DURING ITS EXECUTION OF THE COMMAND. EXCEPTIONS OCCURE WHEN THE DMA ENCOUNTERS Rx END-OF-FRAME BEFORE THE TRANSFER COUNT HAS BEEN SATISFIED AND/OR WHEN ONE OR MORE OF THE BYTES WITHIN A WORD BEING TRANSFERRED ARE NOT VALID (INDICATED BY THE DBYTE(3:0) PINS). A VALUE OF 0x00 INDICATES A BURST SIZE OF 256.

FIG. 12B

FIGURE DMA COMMAND QUEUE ILLUSTRATION

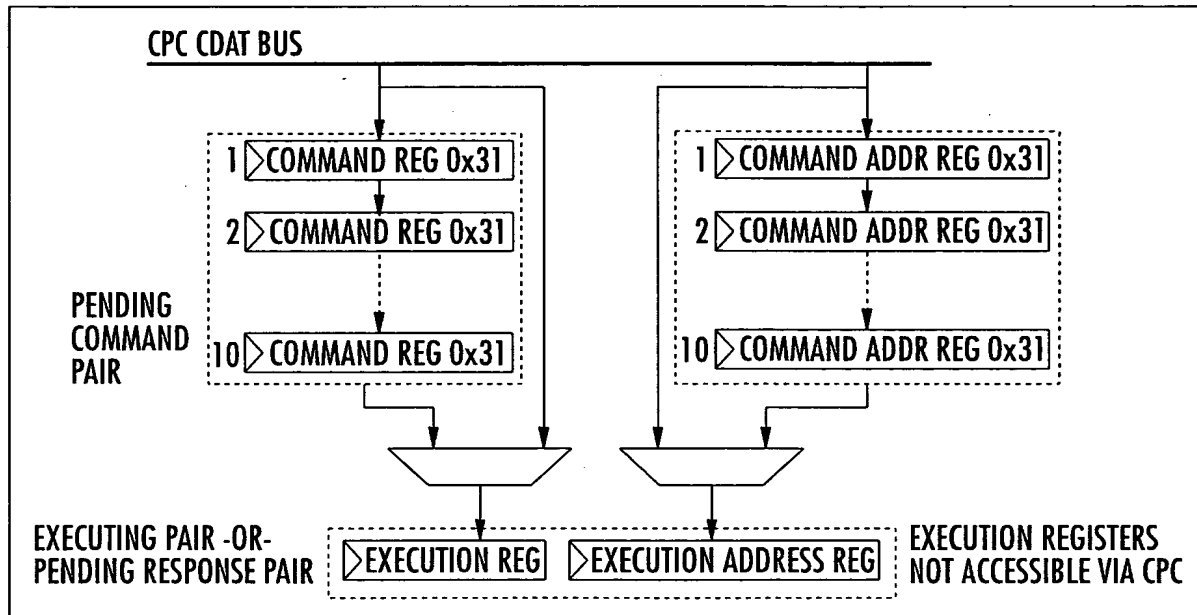


FIG. 13